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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/491,900	01/27/2000	M. Jason Welch	10991989-1	9214

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EXAMINER
NGUYEN, DILINH P

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/491,900	Applicant(s) WELCH ET AL.	
	Examiner DiLinh Nguyen	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,17,18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,17,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 and 17-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) in view of Yoshitake (U.S. Pat. 6043704).

- Regarding claims 1 and 17, Applicant Admitted Prior Art disclose an integrated circuit (Figs. 1 and 2) comprising:

a first port 10-13 for outputting a signal;

a second port 14, 15, 16 and 17 for receiving the signal;

a common area 35 comprising an alignment link 30, 31, 32 and 33 for electrically connecting the first port with the second port;

the second port extends directly into the common area from a second area;

the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port. However, Applicant Admitted Prior Art (Figs. 1 and 2) fail to disclose the first port extends directly into the common area from a first area.

Yoshitake discloses a clock distribution circuit for a semiconductor integrated circuit comprising:

an input driver 11 for outputting a signal; a buffer 12 for receiving an output of the driver 11 (fig. 1, column 7, lines 10-20), wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant Admitted Prior Art (Figs. 1 and 2) to provide the driver 11 extends directly from the first area into the buffer 12, as shown by Yoshitake to make a direct contact and avoid the links.

- Regarding claims 2 and 3, Applicants' prior art Figure 2 discloses the alignment link comprises a wiring trace and a common area 35 of integrated circuit real estate.
- Regarding claims 4 and 5, Applicants' prior art Figure 1 discloses the first port and second port are located in a first and second area respectively of integrated circuit real estate.
- Regarding claim 18, Applicants' prior Fig. 2 discloses the alignment means comprises a wiring trace and signal buffering circuitry and occupy a common area 35 of integrated circuit real estate.
- Regarding claim 20, Applicants' prior art Fig. 2 discloses the first port and second port are located at a substantial distance to each other relative to overall integrated circuit estate.

3. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) in view of Yoshitake (U.S. Pat. 6043704) and further in view of Mizuno et al. (U.S. Pat. 6140686).

- Regarding claims 6 and 7, Applicant Admitted Prior Art disclose an

integrated circuit (Figs. 1 and 2) comprising:

a first port 10-13 located in a first area of integrated circuit real estate, for outputting a signal;

a second port 14, 15, 16 and 17 located in a second area of integrated circuit real estate, for receiving the signal;

a common area 35 comprising an alignment link 30, 31, 32 and 33 for electrically connecting the first port with the second port;

the second port extends directly into the common area from a second area;

the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port. However, Applicant Admitted Prior Art (Figs. 1 and 2) fail to disclose the first port extends directly into the common area from a first area.

Yoshitake discloses a clock distribution circuit for a semiconductor integrated circuit comprising:

an input driver 11 located in a first area of integrated circuit real state, for outputting a signal; a buffer 12 (fig. 1, column 7, lines 10-20), wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant Admitted Prior Art (Figs. 1 and 2) to provide the driver 11 extends directly from the first area into the buffer 12, as shown by Yoshitake to make a direct contact and avoid the links.

Applicants' prior art (figs. 1-2) and Yoshitake fail to disclose the integrated circuit real estate comprises multi-levels. Mizuno et al. disclose the integrated circuit (Figs. 1, 21 and abstract) comprises multi-levels wherein the multi-levels comprise a semiconductor level and a wiring level, the semiconductor level forms a buffer and control circuit so that the frequency of the oscillation output corresponds to the frequency of the clock signal (abstract) and the wiring levels 110,111, 112, 113 (column 2, lines 55-61) provide the power supply voltage to the circuit block 300 (Fig. 1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ICs of Applicants' prior art (figs. 1 and 2) and Yoshitake such that the integrated circuits real estate comprise multi-levels to maintain the frequency of the signal from the clock to the oscillation and provide the power supply voltage to the circuit block shown by Mizuno et al.

- Regarding claim 8, Mizuno et al. disclose the semiconductor level comprises the signal buffer (abstract).
- Regarding claim 9, the limitation that the wire-tracing level comprises the first port and second port is a design choice.
- Regarding claim 10, Mizuno et al. disclose the wiring level comprises a plurality of wiring levels 110, 111, 112 and 113 (Figs. 1 and 21, column 2, lines 55-61).

Response to Arguments

The Examiner uses the new prior art to reject the claimed invention. Therefore, see the new rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, OLIK CHAUDHURI can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
July 20, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800